WHAT IS CLAIMED IS:

1. A non-volatile memory device comprising:

a substrate;

a plurality of isolation layers on the substrate that define a plurality of active regions therebetween;

a charge storage insulator on the plurality of active regions and the plurality of isolation layers;

a plurality of word lines on the charge storage insulator and crossing over the plurality of active regions; and

a plurality of conductive patterns disposed between at least some of the word lines that penetrate the charge storage insulator to electrically connect with at least some of the plurality of active regions.

2. The non-volatile memory device of Claim 1, wherein a top surface of each of the plurality of isolation layers is disposed farther above the substrate than a top surface of each of the plurality of active regions.

3. The non-volatile memory device of Claim 1, wherein the charge storage insulator comprises a multi-layer structure having at least one oxide layer.

4. The non-volatile memory device of Claim 3, wherein at least one of the at least one oxide layers comprises an insulating metal oxide layer.

5. The non-volatile memory device of Claim 1, wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer disposed on the lower oxide layer and an insulating metal oxide layer disposed on the charge trapping layer.

6. The non-volatile memory device of Claim 1, wherein the plurality of isolation layers and the plurality of active regions are located in a cell region of the device and wherein the charge storage insulator is on substantially the entire surface of the cell region.

7. A non-volatile memory device comprising:

a substrate having a cell region, a high voltage region and a low voltage

region;

a plurality of trench isolation layers on the substrate that define a plurality of first active regions in the cell region, a plurality of second active regions in the high voltage region and a plurality of third active regions in the low voltage region;

a charge storage insulator on the plurality of first active regions and the plurality of trench isolation layers in the cell region of the device;

a plurality of gate lines on the charge storage insulator and crossing over the plurality of trench isolation layers in the cell region of the device.

8. The non-volatile memory device of Claim 7, the device further comprising:

a high voltage gate electrode crossing over each of the plurality of second active regions and a first insulation layer interposed between the high voltage gate electrode and each of the plurality of second active regions.

a low voltage gate electrode crossing over each of the plurality of third active regions and a second insulation layer interposed between the low voltage gate electrode and each of the plurality of third active regions.

9. The non-volatile memory device of Claim 7, wherein a top surface of each of the plurality of trench isolation layers is disposed farther above the substrate than a top surface of each of the plurality of first, second and third active regions.

10. The non-volatile memory device of Claim 7, wherein the charge storage insulator is a multi-layer structure that includes an insulating metal oxide layer.

11. The non-volatile memory device of Claim 8, wherein the first insulation layer is thicker than the second insulation layer.

12. The non-volatile memory device of Claim 11, wherein the first insulation layer comprises a first oxide layer and a lower oxide layer and wherein the second insulation layer comprises a second oxide layer and a lower oxide layer.

13. The non-volatile memory device of Claim 12, wherein the plurality of gate lines include a plurality of word lines, a ground selection gate line and a string selection gate line and wherein the second oxide layer is further interposed between

the charge storage insulator and the first active region at the regions of the charge storage insulator that are under the ground and string selection gate lines.

14. The non-volatile memory device of Claim 8, wherein the first insulation layer comprises a first oxide layer, a lower oxide layer and a second oxide layer and wherein the second insulation layer comprises the lower oxide layer and the second oxide layer.

15. The non-volatile memory device of Claim 14, wherein the first insulation layer and the second insulation layer each further comprise an upper oxide layer on the second oxide layer.

16. The non-volatile memory device of Claim 13, wherein a lower oxide layer is further interposed between the string selection gate line and the plurality of first active regions, and between the ground selection gate line and the plurality of first active regions.

17. The non-volatile memory device of Claim 8, wherein the first insulation layer comprises a first oxide layer and a second oxide layer and wherein the second insulation layer comprises the second oxide layer.

18. The non-volatile memory device of Claim 17, wherein each of the plurality of gate lines comprises a second conductive layer and a third conductive layer and wherein the high and low voltage gate electrodes comprise a first conductive layer and a third conductive layer.

19. A non-volatile memory device comprising:

a substrate having a cell region, a high voltage region and a low voltage region;

a plurality of device isolation layers on the substrate that define a plurality of first active regions in the cell region, a second active region in the high voltage region and a third active region in the low voltage region;

a charge storage insulator disposed on the first active regions and the plurality of device isolation layers wherein the charge storage insulator comprises a lower oxide layer, a charge trapping layer and an upper oxide layer;

a plurality of gate lines on the charge storage insulator that cross over the

plurality of device isolation layers;

a first gate electrode crossing over the second active region;

a second gate electrode crossing over the third active region;

a first insulation layer interposed between the first gate electrode and the second active region; and

a second insulation layer interposed between the second gate electrode and the third active region.

20. The non-volatile memory device of Claim 19, wherein the plurality of gate lines include a plurality of word lines disposed in a word line portion of the cell region, and a ground selection gate line and a string selection gate line that are disposed in a selection gate portion of the cell region and wherein the lower oxide layer of the charge storage insulator is thinner under the plurality of word lines than the lower oxide layer of the charge storage insulator is under the ground selection gate line and the string selection gate line.

21. A method of fabricating a non-volatile memory device comprising:

forming a plurality of trench isolation layers in a cell region of a substrate to define a plurality of active regions; and then

forming a charge storage insulator on the plurality of active regions and the plurality of device isolation layers; and

forming a plurality of gate lines on the charge storage insulator that cross over the plurality of device isolation layers.

22. The method of Claim 21, further comprising:

forming conductive patterns that penetrate the charge storage insulator between some of the plurality of gate lines to electrically connect with at least some of the plurality of active regions.

23. The method of Claim 21, wherein the charge storage insulator is formed over substantially the entire surface of the cell region.

24. The method of Claim 21, wherein forming a plurality of trench isolation layers in the cell region comprises:

forming a pad insulation layer and a hard mask layer on the substrate;

patterning the hard mask layer, the pad insulation layer and the substrate to

form a plurality of parallel trenches in the substrate in the cell region; and

forming an insulating layer on the patterned hard mask layer, pad insulation layer and substrate that fills in the plurality of parallel trenches.

25. The method of Claim 21, further comprising:

exposing the hard mask layer by polishing the insulation layer so as to divide the insulation layer into a plurality of trench isolation layers.

26. The method of Claim 25, further comprising removing the hard mask layer and the pad insulation layer after the plurality of trench isolation layers are formed.

27. The method of Claim 21, wherein forming the charge storage insulator comprises sequentially forming a lower oxide layer, a charge trapping layer and an upper oxide layer.

28. The method of Claim 27, wherein the upper oxide layer is formed of insulative metal oxide layer.

29. The method of Claim 21, wherein the trench isolation layers are formed such that the top surfaces of the plurality of trench isolation layers are disposed farther above the substrate than the top surfaces of the plurality of active regions.

30. A method of fabricating a non-volatile memory device comprising:

forming a plurality of isolation layers in a substrate to define a plurality of first active regions in a cell region of the device, a second active region in a high voltage region of the device and a third active region in a low voltage region of the device; and then

forming a charge storage insulator on at least the first active regions;

forming a plurality of gate lines on the charge storage insulator.

forming a first gate electrode over the second active region; and

forming a second gate electrode over the third active region.

31. The method of Claim 30 further comprising:

forming a first insulation layer on the second active region prior to forming the first gate electrode; and

forming a second insulation layer on the third active region prior to forming the second gate electrode.

32. The method of Claim 31, wherein forming the first insulation layer comprises forming a first oxide layer on the second active region followed by forming a lower oxide layer on the first oxide layer; and

wherein forming the second insulation layer comprises forming a second oxide layer that is thinner than the first oxide layer on the third active region followed by forming the lower oxide layer on the second oxide layer.

33. The method of Claim 30, further comprising:

forming conductive patterns that penetrate the charge storage insulator between some of the plurality of gate lines to electrically connect with at least some of the plurality of first active regions.

34. The method of Claim 33, wherein the charge storage insulator is formed over substantially the entire surface of the cell region.

35. The method of Claim 30, wherein forming a plurality of isolation layers comprises:

forming a pad insulation layer and a hard mask layer on the substrate;

patterning the hard mask layer, the pad insulation layer and the substrate to form a plurality of trenches in the substrate; and

forming the plurality of isolation layers that fill in the plurality of trenches.

36. The method of Claim 35, wherein forming the plurality of isolation layers comprises forming an insulation layer over substantially the entire surface of at least the cell region and then exposing the hard mask layer by polishing the insulation layer so as to divide the insulation layer into the plurality of isolation layers.

37. The method of Claim 36, further comprising removing the hard mask layer and the pad insulation layer after the plurality of isolation layers are formed.

38. The method of Claim 30, wherein forming the charge storage insulator comprises sequentially stacking a lower oxide layer, a charge trapping layer and an upper oxide layer, and wherein the upper oxide layer is formed of insulating metal oxide layer.

39. The method of Claim 30, wherein the isolation layers are formed such that the top surfaces of the plurality of isolation layers are disposed higher than the top surfaces of the plurality of first active regions.